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Resistive Switching in the Cu/Si/SiO_2/CdS/CuO/Cu Structure Fabricated at Room Temperature Haneafa Yahya Najm

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ABSTRACT

This work investigates CuO and CdS (material as nanoparticles mixed with a polymer (Cellulose Acetate)) – based ReRAM having stable resistive switching. It also investigates a new composition of a memory which is constructed with silicon as a pedestal, silicon oxide SiO_2 thermally grown on it and active materials that include of (CuO material as nanoparticles mixed with a polymer (Cellulose Acetate) layer) sandwiched between two electrodes using similar material and CdS layer as a semiconductor n-type. ReRAM memory cell is a structure such as a capacitor that is consist of semiconducting transition metal oxides or insulating exhibiting inverses resistive switching on applying voltage pulses .The mixed material was coated as a thin layer by using Spin-Coating Instrument. this structure can be switched between low-resistance state (LRS) and high resistance state(HRS);therefore, The present structure behaves as unipolar resistive switching. The resistive behavior will be affected by the top electrode area. This effect occurs more in big top electrode area (TEL=15.896mm^2) where, the constituting voltage ($V_{forming}$) is inversely proportionately with respect to the top electrode area (A) .Also the (HRS) is inversely proportioned with the (A). The complying current (Icc=20mA) is used for protect the device from the damageable. The fabricated composition has many prosperities, such as $V_{forming}$ = 7.3volt, V_{set} = 4volt, V_{Reset} = 1.7volt, Finally, the resistance ratio (R_{ratio}) is proportioned directly with the(A) and equal R_{ratio}=157.48 so, this ratio is enough to distinguish amongst the low resistance and the high resistance in a circuit design.

Introduction

There are two kinds of wantonly access memory (RAM): volatile and nonvolatile. When power is eluting, stored data is lost in the volatile memory as in static wantonly access memory (SRAM) [1]. Whereas, in nonvolatile memory, The stored data is not lost when disconnecting source energy.

Memory devices have benefits and weaknesses. For example, Dynamic random-access memory (DRAM) is widely used in digital electronics where low-cost and high-capacity memory is required[2,3]. Static random access memory (SRAM) loses its content when powered stopping, and is categorized as volatile memory. Popular Flash memory is nonvolatile and has a very high capacity, Yet it is relatively slow [4]. Besides being nonvolatile, an ideal memory would have a fast allergy, long retention time, high capacity, and low power consumption, and scaling better than present technologies. Recently ,scholars have been enthusiastically studying emerging nonvolatile Memory (NVM) technologies like Phase Change (PCRAM), Magnetic (MRAM) and Resistive (RRAM) will possibly enable memory chips that are non-volatile, require low-energy and have density and latency closer to current DRAM chips [5]. Among these nominees, Resistive random access memory (ReRAM) contain a simple instrument of a structure consists of metal–insulator–metal (MIM) is considered one of the promising future device for different applications liker nonvolatile data storage [6]. Therefore, more interests is being concentrated on these devices. Re-RAMs have been lately confirming their devices. due to their potential for

down scaling and dipped-power consuming, Re-RAMs have been lately settling their consideration as appearing technology by the International Technology Roadmap for Semiconductors [7]. Resistive switching phenomenon has been firstly studied in 1970s and 1980s. the first researches mostly concentrated on debating and reagent the physical mechanism of electrical catalyzed resistive switching. With the sophistication of microelectronics processing technology, researchers acknowledged that resistive switching demeanor can be used as an finality nonvolatile memory in the late 1990s, bringing the second research flow of resistive switching [8] ReRAM is generally made of a metal-insulator-metal structure, typically using transition metal oxides as the insulator [9] and organic compounds[10] and some nanoparticles from metal or semiconductors within some polymers to fabricated electrical stable devices [11] which appear a resistive switching phenomenon. The ReRAM memory cell includes a capacitor such as structure inserted between two metal electrodes (Fig1). A large alter in resistance (>1000%) occurs on implementing pulsed voltages in the resistive switching phenomenon (Fig.1). By applying the appropriate voltage pulse, the resistance of the cell can be set to desired values[9]. A new monograph has revealed that the pace of switching can be quicker than several nanoseconds[12].Oxide materials have been measured intensively among the substance that shows a resistive switching phenomenon in 1962, Hickmott [13].first stated hysteretic current–voltage (I–V) characteristics in metal-insulator-metal (MIM) construct of Al-Al_2O_3-Al, which indicates that resistive switching happens just as a outcome of applied electric field. Resistive switching has afterwards been indicated in a vast assorted of MIM structures composed of binary metal oxides, like SiO[9]. ReRAM researches involved different switching demeanor such as unipolar phenomenon and bipolar phenomenon, different switching mechanisms like trap controlled model[15], filament model[14], interface barrier model[16] and Mott transition[17]. Many current monographs have provided indirect evidence for the constitution of conductive filaments within the dielectric [18], for instance, it was reported that the resistance of the low resistive state LRS does not rely on the area of the metal electrode. Whilst that of the high resistance state HRS scales adversely with the electrode area [19]. This means that the current gushing should be spatially inhomogeneous in the LRS but not in the HRS [20].The aim of this research is to obtain the lowest operating voltage of the cell.

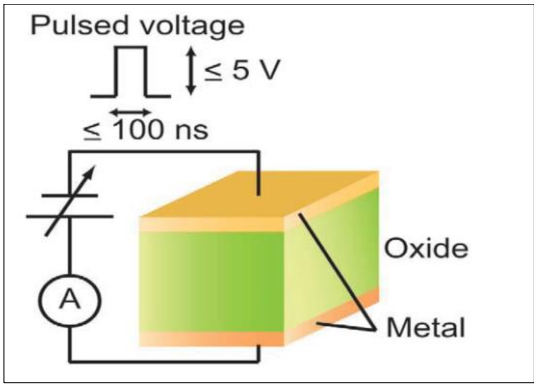

Fig. 1: Diagram of a ReRAM memory cell with a capacitor-like structure in which an insulating or semiconducting oxide is sandwiched between two metal electrodes[6]

I. Classification of resistive switching

II. I Unipolar and Dipolar resistive switching

The operation from LRS to HRS is dubbed the RESET process, whilst, the switching operation from HRS to LRS is dubbed the SET process. Ordinarily, for new specimens in its initial resistance state, a voltage must be larger than the SET voltage is coveted to the ordinance the transition from HRS to LRS than the suffix cycles. This operation is dubbed the FORMING process. The FORMING/SET process is completed when the current in the ordinance getting equal to the compliance current (Icc) level. Depending on the relative polarities of the SET and RESET voltage, the resistive switching phenomenon is called either unipolar or dipolar (Fig. 2) [9].

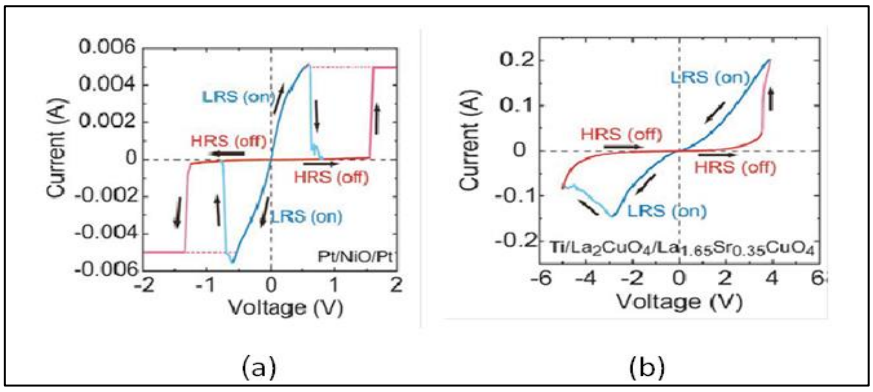

Fig.2: I - V curves during different type of resistive switching: (a) unipolar switching in a Pt/NiO/Pt cell and (b) bipolar switching in a Ti/La2CuO4/La1.65Sr0.35CuO4 cell. [9].

II. II MECHANISMS OF RESISTIVE SWITCHING

There are two kinds of mechanism resistive switching for ReRAM: filament and interface which are schematically shown in (Fig.3), respectively [9]. In the filament model, the resistance switching takes place owing to the rending and formation of localized conductive filament (CF) in the sandwiched dielectric layer also termed as switching layer upon the application of suitable external electrical stimulus as shown Fig. 3(a), whereas in the interface kind mechanism, the switching take place at the interface of the metal and switching material owing to the movement of ions, oxygen vacancies or detrapping trapping and of electrons or eyelets infra the applied electric field Fig. 3(b)[9] .

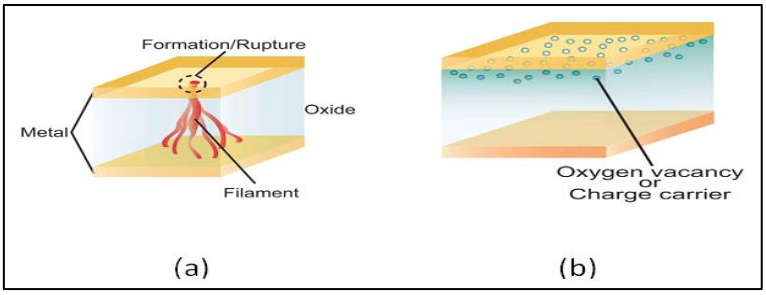

Fig. 3: Schematics (a) resistive switching of a filament conducting track, (b)resistive switching of an interface. conducting track. [9].

Utilization of Nanoparticles in the recent Memories:

Recently, to fabricate electrically bitable devices, some combos enter metal or semiconductor nanoparticles into polymers and a notable electrical constancy was attained in these devices[21].

various physical and chemical methods have recently been used to study and synthesized Nano particles because of new physical and chemical peculiarities Engineered and designed nano-particles are a catchier choice in deferent environmental applications. As the peculiarities of nano-materials differ from the bulk phase, it can impact their application in heterogeneous catalysis [22].

Iv. Experiments

To construct the present structure, the wafer of silicon p-type < 100 > is used as a substrate and prepared using a special cleaning process. The second step after cleaning the substrate is the oxidation using a furnace with maximum temperature (1200°C) to make thermal oxidation see figure (4) of thickness 75 Å which was measured by Electroscopic Reflectometer Instrument. The next step after thermal oxidation is the depositing a thin layer of Cadmium Sulfide CdS with thickness (600 Å) by using the thermal evaporation system (the Balzer system).The CdS thin film here represents n-type semiconductor. After the depositing process of CdS, the CuO as metal oxides nanoparticles are coating on CdS layer by using Spin-Coater Instrument type (INSTRAS, sck-100 spin coater kit) by mixed it with a polymer material (Cellulose Acetate) for thickness about 2000Å see figure(5). The final step for fabrication of the structure is the depositing thin layers of metal (Cu) with the thickness of about (3000 Å) as Top Electrodes (TEs) for three areas (15.896 mm^2, 4.906 mm^2 and 3.14 mm^2) on the CdS layer by using thermal evaporation system (the Balzers BA 510) and special masks see figure (6). The bottom electrode is fabricated by depositing (Cu) metal about (3000 Å) on the other face of the wafer see figure (7). Finally, The structures are tested with AC and DC sources using a maximum current of (Icc = 20mA) as to compliance current.

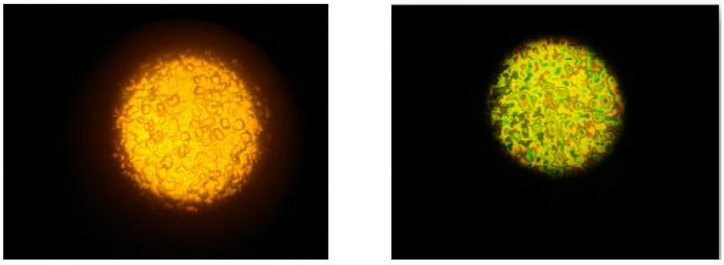

Fig. 4: The wafer of p-type silicon with amplification by 600 times for the internal composition of the (a) before the thermal oxidation (b) after cleaning and thermal oxidation with maximum temperature (1200°C).

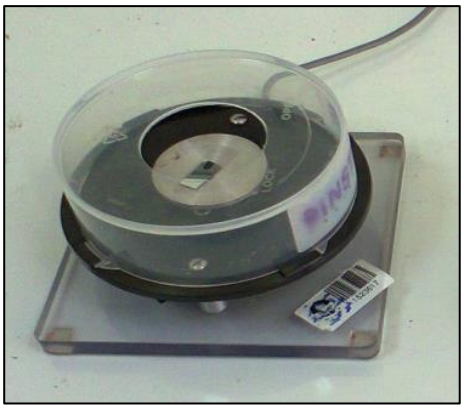

Fig. 5: The images of The Spin-Coater for thin films polymers.

Fig. 6: The mask shape for fabricated structure.

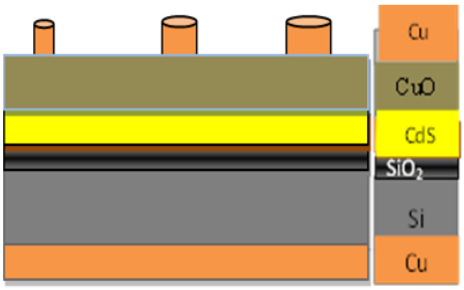

Fig. 7: The cross section of the structures.

V. Results and discussion:

V.I. Testing the Devices using DC measurements:

The DC testing of memory can be achieved by using (I-V) properties of the fabricated device were measured by (KEITHLEY 6487 PICOAMMETER / VOLTAGE SOURCE) for three states:

a) With large Top Electrode (TEL), the area is AL= 15.896 mm^2.

b) With medium Top Electrode (TEm), the area is Am= 4.906 mm^2.

c) With Small Top Electrode (TES), the area is AS= 3.14 mm^2.

As the $V_{forming}$ was practically measured by a voltmeter directly when the cell was manufactured.

Through the result of DC (I-V) characteristics, it Appears that the symmetry concerning the origin for two bias of positive and negative voltage are equal, since the cell is unipolar So, the positive bias will be enough for studying the resistive switching of the device as explained in the figure (8).

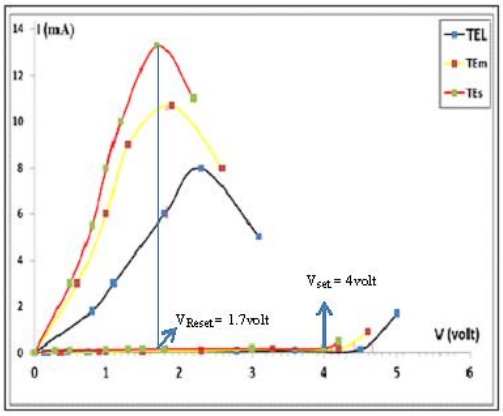

Fig. 8: (I-V) properties for the device with CuO coating for many electrodes areas using compliance current I_{cc}=20mA.

From figure (8), the values of voltages $V_{forming}$,V_{set} , V_{Reset} and the resistance of the device in case of low resistance switching (RLRS)) in case of TES will be higher than those values in case of TEm and TEL respectively. While the resistance of the device in case of high resistance switching (RHRS) are inversely proportional with changing of the area of the top electrode, this congruously with conclusions the researcher Seo and et al., for resistive switching [23]. Finally, the compliance current (Icc) are utilized for conservation the device from perishable, So, this equal to Icc= 20mA.Table (1-1) summarizes the changing of the above values. The above Structures behave Unipolar resistive switching. This may happen because the structure uses the same material (Cu) as top and bottom electrodes [24].

Table (1-1) summary for the important measured parameters for the device with CuO coating for many tops electrodes areas.

Table 1-1: there are present inversely proportional between the top electrode area (A) with forming voltage $V_{forming}$ for the device. So, this relation can be drawing as shown in figure (9).

	TE_L	TE_m	TE_S
$V_{Forming}$	7.3V	7.9V	8.1V
V_{Set}	4V	4.2V	4.5V
V_{Reset}	1.7V	1.9V	2.3V
R_{HRS}	20KΩ	23.33KΩ	30KΩ
R_{LRS}	0.127KΩ	0.177KΩ	0.287KΩ
R_{atio}	157.48	131.8	104.52

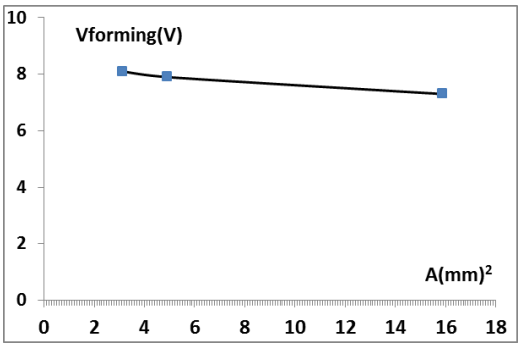

Fig. 9: The relation between A and $V_{forming}$ for many devices with CuO coating.

Also, from table (1-1), there are direct relation between A and R_{ratio} for the device with CuO coating as shown in figure (10).

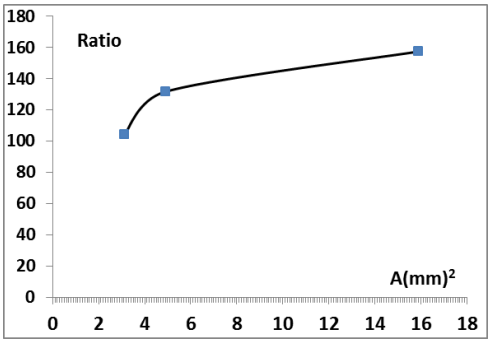

Fig. 10: The relation between A and R_{ratio} for the device with CuO coating.

The Resistance ratio, plays an important role in ReRAM implementations owing it directly impacts the exactitude of programming and erasing. At least , a resistance ratio greater than 10 is obligatory to difference the two resistance conditions in circuit design [25]. The resistance ratio can be as high as six or seven orders of magnitude In some ReRAM devices, [26]. So, the best structure, reveals a chunkier resistance ratio.

The resistor endurance of the device with CuO coating in the case of TEL was studied as shown in figure (11). From this figure, there are about two orders of magnitude between the high resistance state (HRS) and low resistance state (LRS).

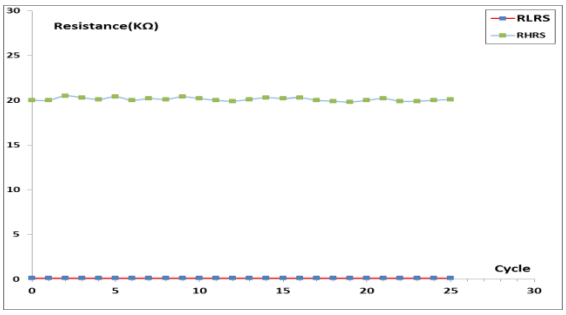

Fig. 11: Endurance for resistance LRS and HRS of the device with CuO coating in case of TEL.

In same manner, the voltage endurance (V_{set} and V_{Reset}) of the device with CuO coating in case of TEL can be achieved as shown in figure(12).

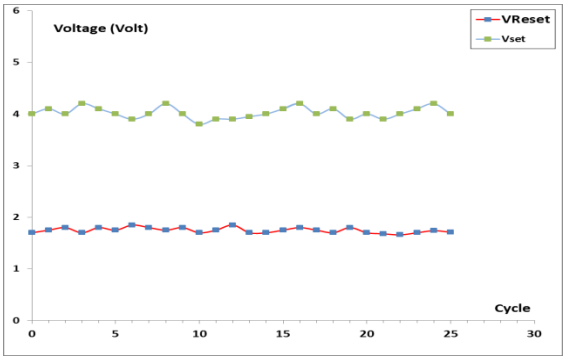

Fig. 12: Endurance of the voltages (V_{set} and V_{Reset}) of the device with CuO coating in case of TEL.

V.II. Testing the Devices using AC Measurements:

The AC testing of memory can be achieved, by using (I-V) properties of the fabricated devices. The measurements were fulfilled using Storage Digital Oscilloscope type (OWON MSO 7102T) and Function Generator type (PHILIPS PM 5127 0.01Hz – 1MHz) giving triangle pulses.

From AC testing, the following can be determined:

Resistance Ratio Measurement (R_{ratio}):

These measurements can be achieved by drawing between (I-V) for the device under test (DUT), where channel 1 (ch1) represented the voltage across DUT and channel 2 (ch2) represented the current through DUT by dividing the voltage across DUT on R=100Ω . So, figure (13) represents the AC measurements in the case of TEL.

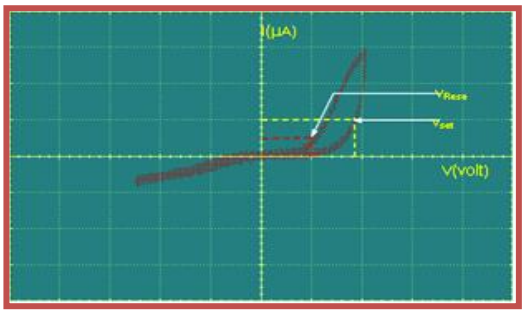

Fig. 13: The AC measurements of the device with CuO coating in case of .

$$R_{HRS} = R_{off} = \frac{4V}{0.2mA} = 20K\Omega$$

$$R_{LRS} = R_{on} = \frac{1.7V}{13mA} = 0.13K\Omega$$

$$R_{ratio} = \frac{R_{HRS}}{R_{LRS}} = \frac{R_{off}}{R_{on}} = \frac{20K\Omega}{0.13K\Omega} = 153.846$$

One can be observed that The values of the parameters R_{HRS}, R_{LRS}, R_{ratio}, V_{set} and V_{Reset} in AC measurements are nearly equal to DC measurements of the device with CuO coating in case of TEL.

By AC measurements, the Switching Time Measurement (Ts) of the device with CuO coating can be calculated in the case of TEL. So, from the figure(13) the Switching Time is calculated as:

$$T_s = \frac{1}{f_s} = \frac{1}{9.2kHz} = 108.695\mu sec = 108695\ ns.$$

V.III. Scanning electron microscope (SEM) Measurements:

The SEM measurement for the device with CuO, see figure (14).

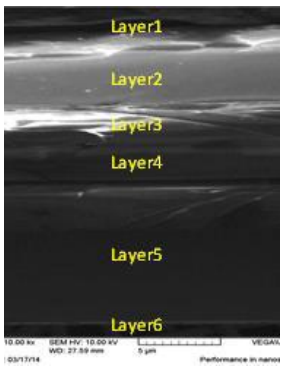

Fig. 14: Cross - sectional scanning electron microscopy (SEM) images for the device with CuO coating.

The SEM image (figure 14) reveals six layers. Layers (1 and 6) represent the top and bottom metal electrodes (Cu) respectively, while layers (5 and 4) represent the cross section silicon wafer and the silicon oxide which is grow thermally on the silicon substrate ,while the layer (3) is the active martial CdS which represents the n-type semiconductor deposited on the silicon oxide, finally the layer (2) represents the CuO mixed with Polymer martial (Cellulose Acetate).while, the SEM image (figure 15) reveals the CuO in micrometers which is equal 10^3 nanometer.

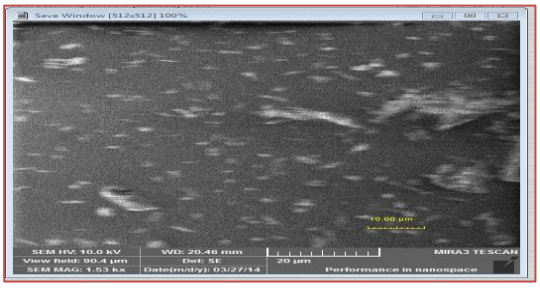

Fig. 15: SEM image for CuO in (10.00) micrometers and equal (10^4) nanometer .

VI. Conclusions

We noticed in the research above, that the resistive switching mechanisms of RRAM device can be characterizing through the (I – V) relations, in two cases, DC and AC. The device exhibits the Unipolar (I – V) characteristics, because has isomorphic structure, which implies that the up electrode (TE) using the same material as the down electrode (BE) (Cu). From the experiments, it is clear that the resistance in high resistive state HRS is inversely proportional to the area of the TE. That is to say $V_{forming}$, V_{set} and V_{Reset} for the same structure will change. also, the forming voltage($V_{forming}$) is inversely proportional with respect to the top electrode area (A), this may occur because the availability of local filamentary conducting paths within the zone of this area. also, this represents the same reason which leading to make the Switching Time(Ts) being inversely proportional with respect to the top electrode area(A).Finally, the resistance ratio (R_{ratio}) is directly proportional to the (A). The complying current (Icc=20mA) is used for protecting the device from the damageable. The fabricated structure has many prosperities, such as $V_{forming}$ = 7.3volt, V_{set}= 4volt, V_{Reset} = 1.7volt and R_{ratio} = 157.48 so, this ratio is enough to distinguish amongst the high resistance and low resistance in circuit design.

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التبديل المقاومي في تركيب Cu / Si / SiO_2 / CdS / CuO / Cu مصنعة في درجة حرارة الغرفة

حنيفة يحيى نجم

قسم هندسة تقنيات القدرة الكهربائية ، الكلية التقنية الهندسية/ الموصل ، الجامعة التقنية الشمالية ، العراق

الملخص

في هذه الدراسة، تم تحقيق ذاكرة الوصول العشوائي المقاومي (ReRAM) بالاعتماد على طبقتين فعالتين CdS و CuO كجسيمات نانوية ممزوجة مع مادة خلات السليلوز البوليمرية والتي تملك تبديلاً مقاومياً مستقراً ، تم ايضاً تحقيق تركيبة جديدة لذاكرة مصنوعة من السليكون كقاعدة اساسية (Substrate) حيث تم انماء طبقة من اوكسيد السليكون (SiO_2) حرارياً عليها وكذلك استخدمت المادتين النانويتن الفعالتين من (CdS) و (CuO) الممزوجتين مع البوليمر كطبقتين بحيث تقع هذه الطبقتين بين قطبين معدنيين من النوع نفسه كنوع من اشباه الموصلات نوع n-type، ان تركيب ذاكرة (ReRAM) يشبه تركيب المتسعة والتي تتكون من شبه موصل من اكاسيد معدنية انتقالية او عازل والتي تبدي تبديلاً مقاومياً قابلاً للتغير عند تسليط الفولتية عليها . تم طلاء الطبقة الرقيقة من المادة الممزوجة باستخدام جهاز تقنية الطلاء بالدوران السريع (Spin-Coating Instrument). هذه التركيبة من الممكن ان تتبدل في حالة المقاومة الواطئة (LRS) وحالة المقاومة العالية (HRS) ولهذا السبب تسلك سلوك تبديل مقاومي احادي القطبية (Unipolar). هذا السلوك للمقاومة سوف يتاثر بمساحة القطب العلوي. حيث يحدث اكثر في حالة القطب العلوي الكبير ($TEL=15.896\ mm^2$)، حيث يكون فولتية التشكيل ($V_{forming}$) تتناسب عكسياً مع مساحة القطب العلوي (A). وكذلك (HRS) تتناسب عكسياً مع (A) اما استخدم التيار المحدد (Icc) والذي يساوي (Icc=20 mA) لحماية التركيبة من التلف. تمتلك التركيبة المصنوعة على العديد من الخصائص مثل: ($V_{forming}$ =7.3 volt) ، (V_{set}= 4 volt) و (V_{Reset} = 1.7 volt), واخيراً نجد ان المقاومة النسبية (R_{ratio}) تتناسب طردياً مع (A) وتساوي (R_{ratio}=157.48) وتعد هذه النسبة كافية للتمييز بين المقاومة الواطئة والمقاومة العالية.